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ABSTRACT OF THE DISCLOSURE

An IC chip comprises a chip peripheral portion and a core macro portion. The chip peripheral portion is made up of a plurality of I/O buffers each of which serves as an interface between the IC chip and the outside thereof, and a plurality of pads to which bonding wires are electrically connected. A CPU core block, peripheral blocks, random logic blocks, and a gate array block are placed in the core macro portion. The respective blocks are electrically connected to one another by metal interconnections. The gate array block designed by a gate array system is layout-designed in accordance with a standard cell system or full custom system together with other blocks.

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